What Is Claimed Is:

1. A power semiconductor device having high avalanche capability, said device comprising:

an N^+ doped substrate and, in sequence, N^- doped, P^- doped, and P^+ doped semiconductor layers, said P^- doped and P^+ doped layers having a combined thickness of about 5μm to about 12 μm; and

recombination centers comprising noble metal impurities disposed substantially in said N^- doped and P^- doped layers.

2. The device of claim 1 wherein said P^- doped layer has a thickness of about 4 μm to about 10 μm.

3. The device of claim 1 wherein said P^+ doped layer has a thickness of about 0.1 μm to about 2 μm.

4. The device of claim 1 wherein said P^- doped layer has a dopant level of at least 10^{16} atoms/cm^3.

5. The device of claim 4 wherein said P^- doped layer has a dopant level of about 2.5x 10^{17} atoms/cm^3.

6. The device of claim 1 wherein said P^+ doped layer has a dopant level of at least 10^{18} atoms/cm^3.

7. The device of claim 6 wherein said P^+ doped layer has a dopant level of about 6×10^{19} atoms/cm^3.

8. The device of claim 1 wherein said N^- doped layer has a dopant level of about 10^{14} atoms/cm^3 to about 10^{15} atoms/cm^3

9. The device of claim 1 wherein said N^- doped, P^- doped, and P^+ doped semiconductor layers are epitaxial layers.

10. The device of claim 1 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.

11. The device of claim 10 wherein said noble metal impurities comprise platinum.

12. The device of claim 11 wherein said recombination centers are formed by platinum diffusion through said N^+ doped substrate into said N^- doped and P^- doped layers.

13. The device of claim 11 containing platinum impurities at a concentration of about $1x10^{15}$ to about $1x10^{16}$ atoms/cm^3.

14. The device of claim 13 wherein said concentration of platinum impurities is about $2 x10^{15}$ atoms/cm^3.

15. The device of claim 1 further comprising an N^+ doped region disposed in said N^- doped layer.

16. The device of claim 1 further comprising an N^+ doped region disposed adjacent said P^+ and P^- doped layers.

17. The device of claim 16 comprising a MOSFET or an IGBT power device.

18. A process for forming a power semiconductor device having high avalanche capability, said process comprising:

forming an N^- doped epitaxial layer on an N^+ doped substrate;

forming a P^- doped layer in said N^- doped epitaxial layer;

forming a P^+ doped layer in said P^- doped layer, said P^+ doped and P^-

doped layers having a combined thickness of about 5μm to about 12 μm; and

forming in said P^- doped and N^- doped layers recombination centers comprising noble metal impurities.

19. The process of claim 18 wherein said P^- doped layer has a thickness of about 4 μm to about 10 μm.

20. The process of claim 18 wherein said P^+ doped layer has a thickness of about 0.1 μm to about 2 μm.

21. The process of claim 18 wherein said P^- doped layer has a dopant level of at least 10^{16} atoms/cm^3.

22. The process of claim 21 wherein said P^- doped layer has a dopant level of about 2.5x 10^{17} atoms/cm^3.

23. The process of claim 18 wherein said P^+ doped layer has a dopant level of at least 10^{18} atoms/cm^3.

24. The process of claim 23 wherein said P^+ doped layer has a dopant level of about $6\text{x}10^{19}$ atoms/cm^3.

25. The process of claim 18 wherein said N^- doped layer has a dopant level of about 10^{14} atoms/cm^3 to about 10^{15} atoms/cm^3

26. The process of claim 18 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.

27. The process of claim 26 wherein said noble metal impurities comprise platinum.

28. The process of claim 27 wherein said forming said recombination centers comprises diffusing platinum through said N+ doped substrate into said N^- and P^- doped layers.

29. The process of claim 28 platinum impurities are present in said N^- and P^- doped layers at a concentration of about $1x10^{15}$ to about $1x10^{16}$ atoms/cm^3.

30. The process of claim 29 wherein said concentration of platinum impurities is about $2 x10^{15}$ atoms/cm^3.

31. The process of claim 28 wherein said diffusing is carried out at a temperature of about 940°C.

32. The process of claim 31 further comprises cooling said device to a temperature of about 600°C at a rate of about 3°C/minute.

33. The process of claim 18 further comprising forming an N^+ doped region in said N^- doped layer.

34. The process of claim 18 further comprising forming an N^+ doped region in said P^- doped layer adjacent said P^+ doped layer.